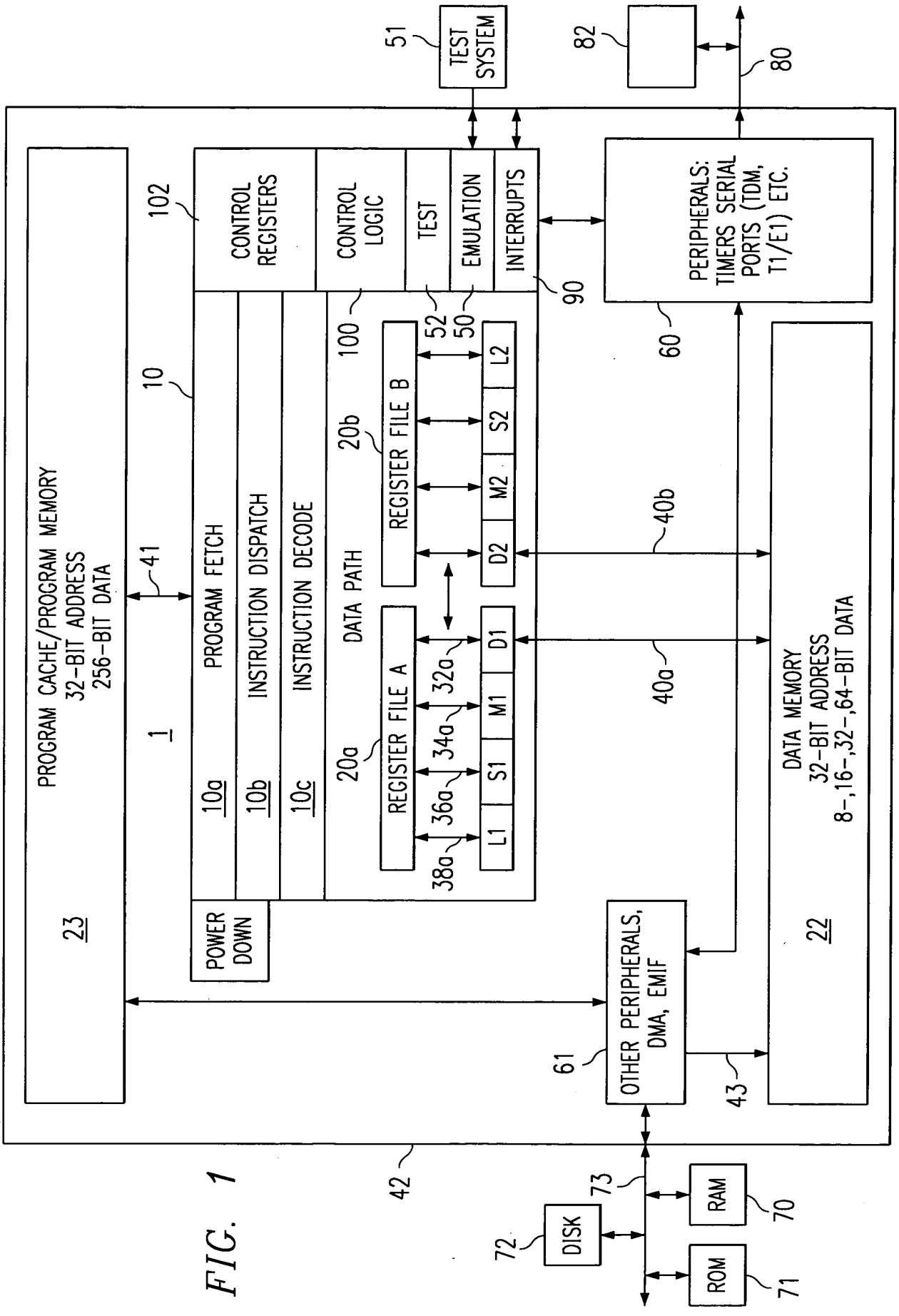

PROGRAM CACHE/PROGRAM MEMORY
32-BIT ADDRESS
256-BIT DATA
23
1
41
10
PROGRAM FETCH
10a
INSTRUCTION DISPATCH
10b
INSTRUCTION DECODE
10c
DATA PATH
100
CONTROL REGISTERS
102
CONTROL LOGIC
TEST
EMULATION
INTERRUPTS
90
52
50
REGISTER FILE B
20b
L2
S2
M2
D2
REGISTER FILE A
20a
L1
S1
M1
D1
32a
34a
36a
38a
40a
40b
POWER DOWN
OTHER PERIPHERALS, DMA, EMIF
61
43
DATA MEMORY
32-BIT ADDRESS
8-,16-,32-,64-BIT DATA
22
PERIPHERALS: TIMERS SERIAL PORTS (TDM, T1/E1) ETC.
60
TEST SYSTEM
51
82
80
42
73
DISK
72
RAM
70
ROM
71

FIG. 1

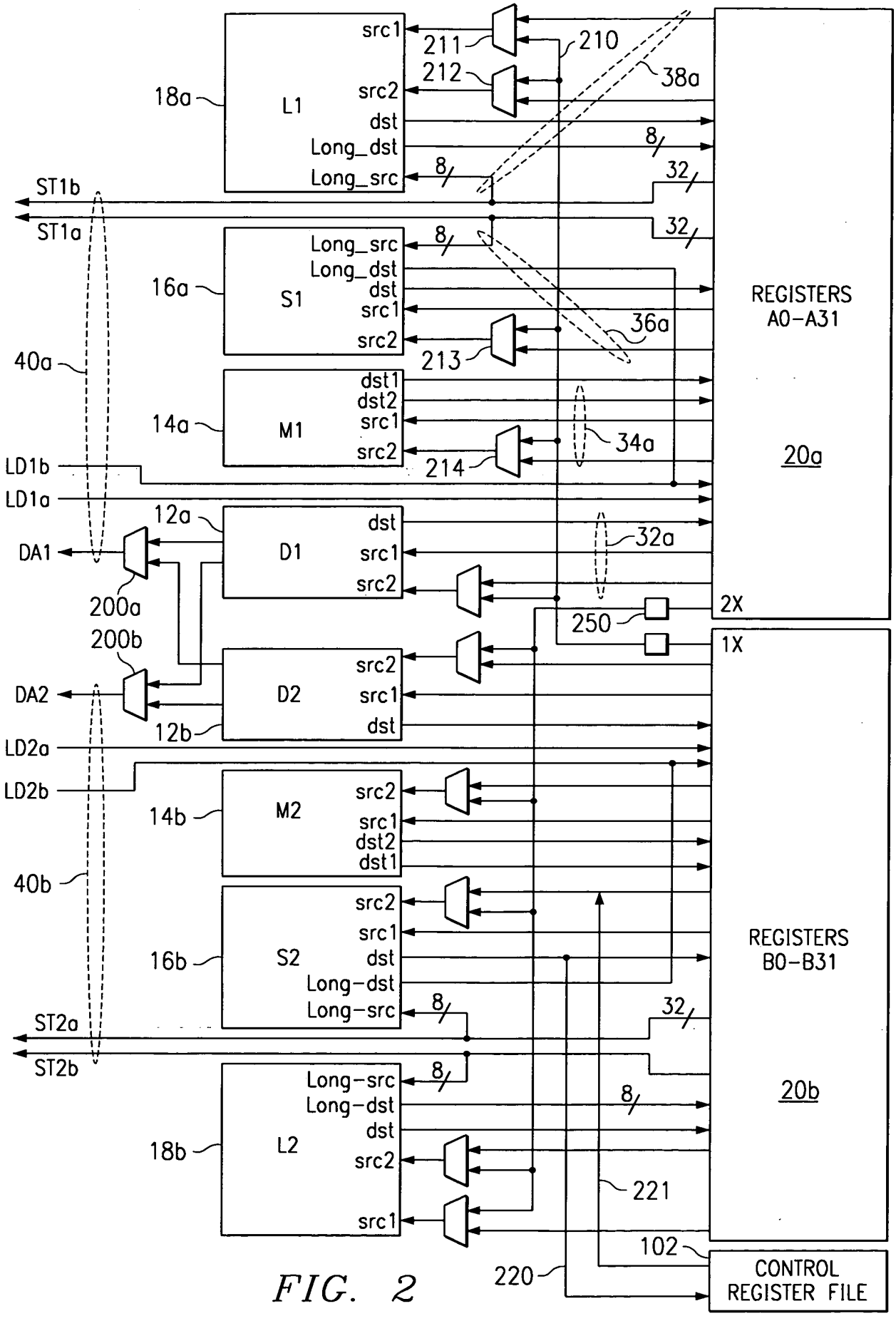


FIG. 2

09/02/2004, 4:08:20 PM

09702320 "10310D

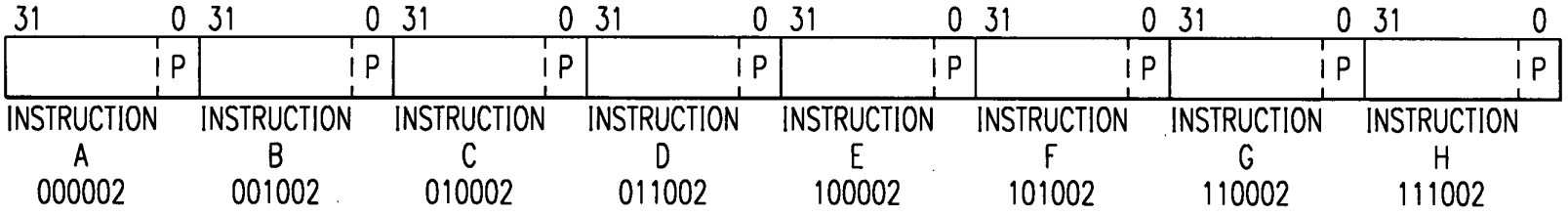


FIG. 3

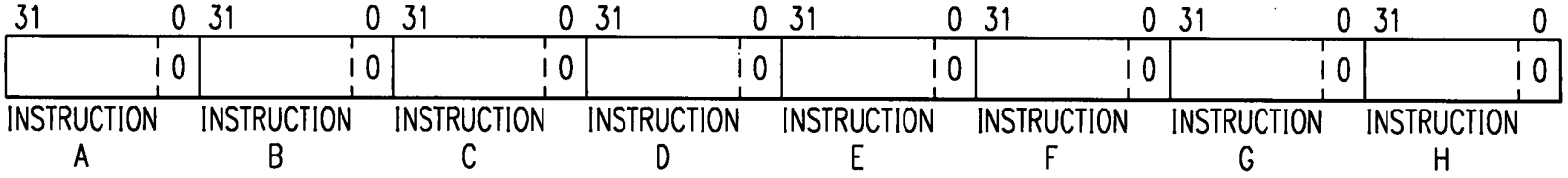


FIG. 4A

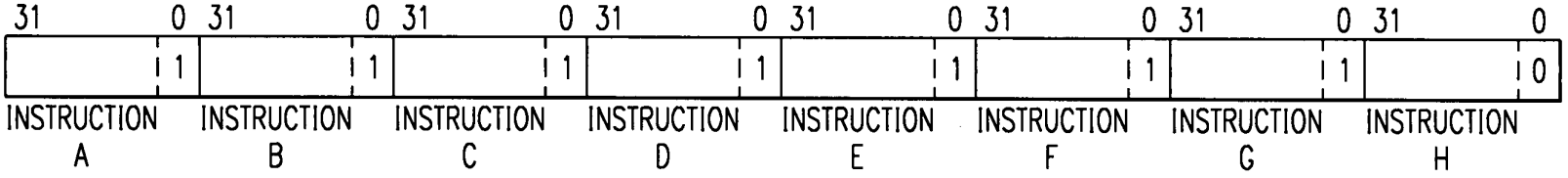


FIG. 4B

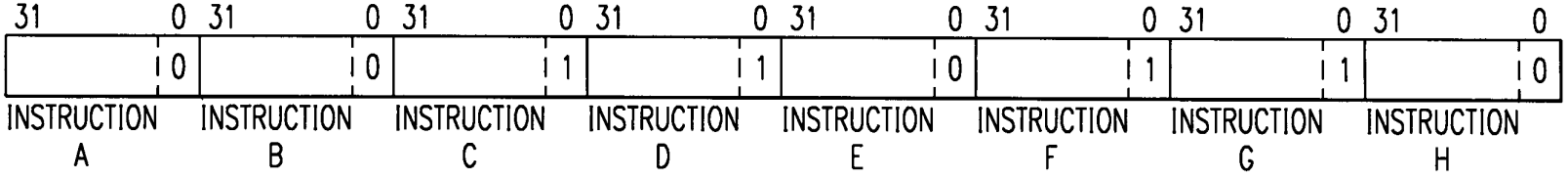


FIG. 4C

FETCH PACKET	EXECUTE PACKET	CLOCK CYCLE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
n	k	PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5												
n	k+1						DP	DC	E1	E2	E3	E4	E5											
n	k+2							DP	DC	E1	E2	E3	E4	E5										
n+1	k+3		PG	PS	PW	PR	PR	PR	DP	DC	E1	E2	E3	E4	E5									
n+2	k+4			PG	PS	PW	PW	PW	PR	DP	DC	E1	E2	E3	E4	E5								
n+3	k+5				PG	PS	PS	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5							
n+4	k+6					PG	PG	PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5						
n+5	k+7								PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5					
n+6	k+8									PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5				

FIG. 5

FIG. 7A
(PRIOR ART)

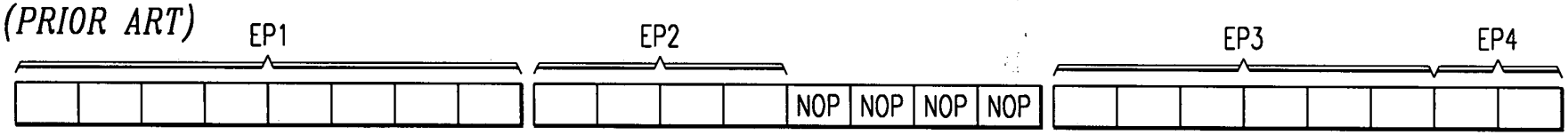
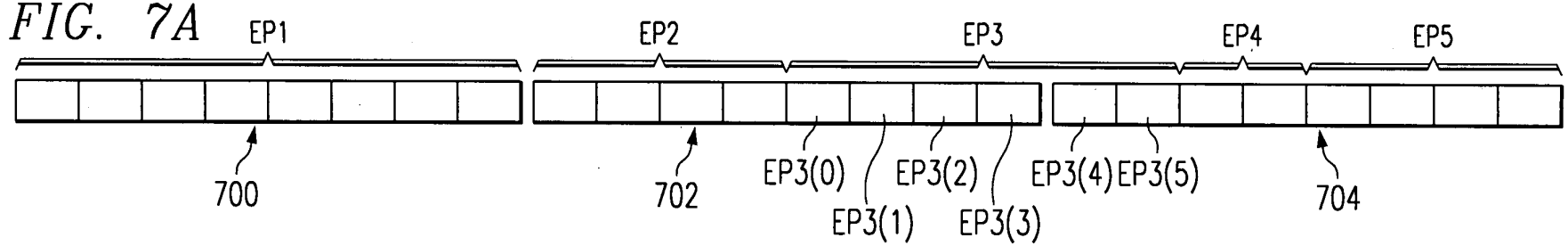


FIG. 7A



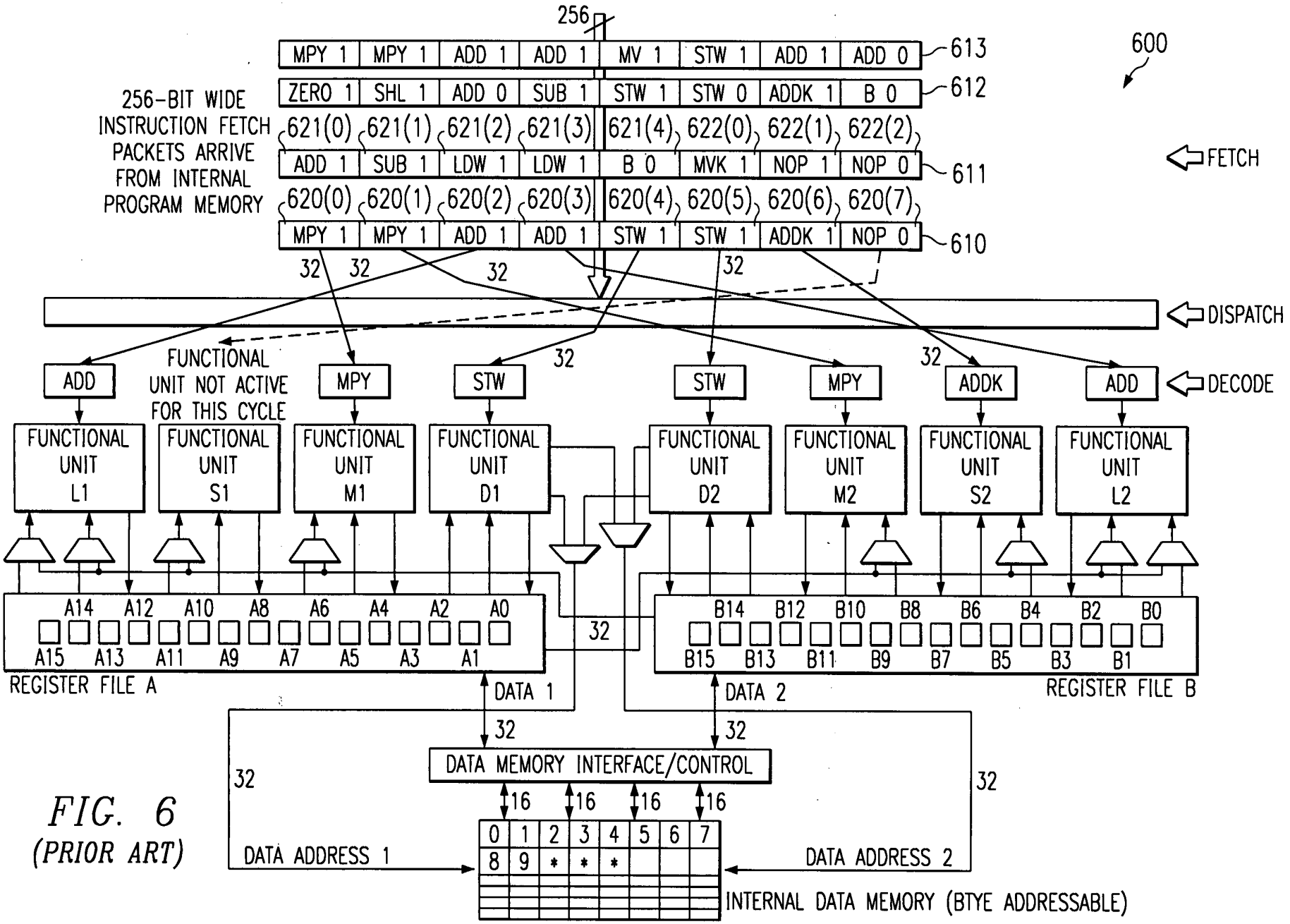


FIG. 6
(PRIOR ART)

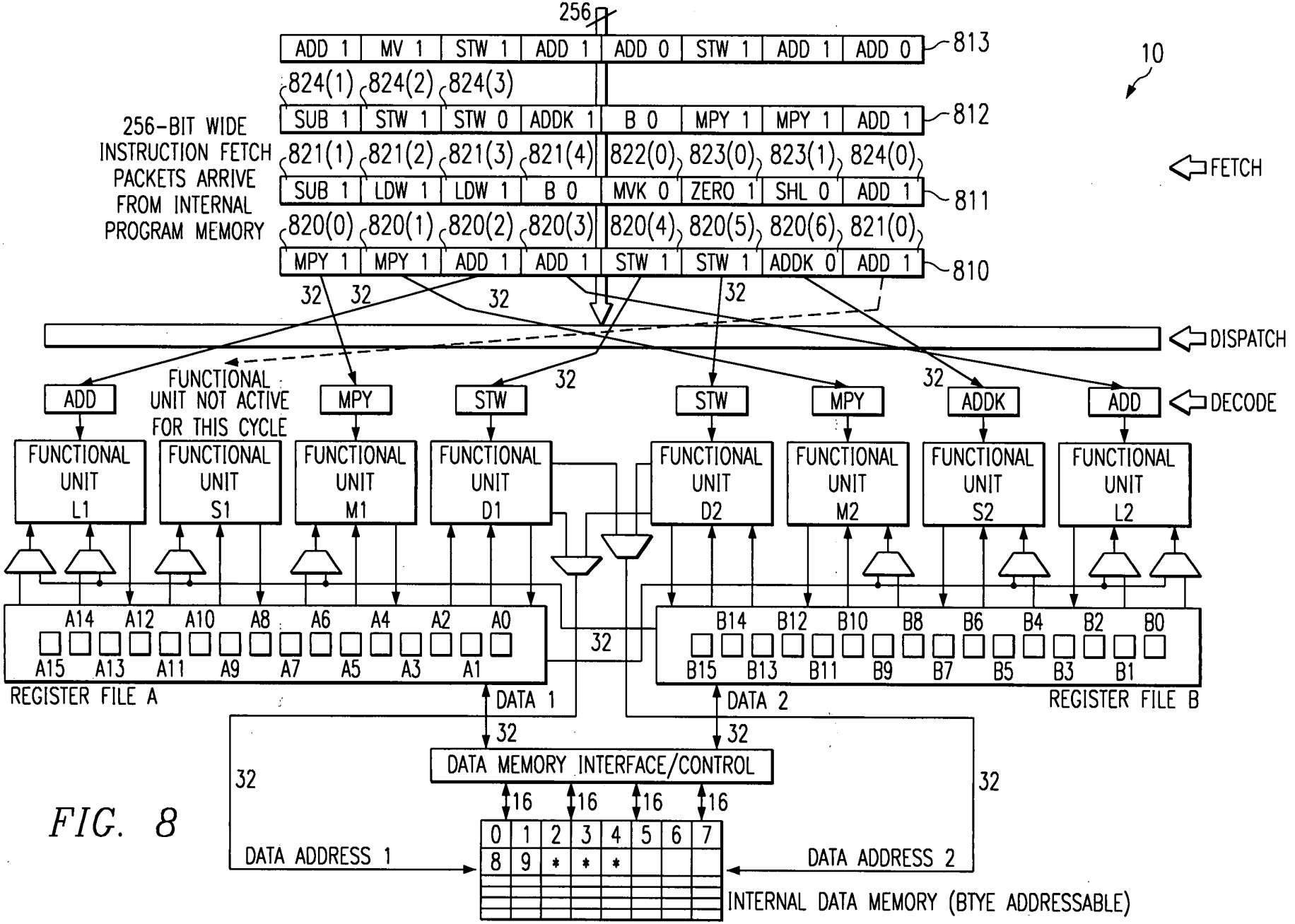

256
ADD 1 | MV 1 | STW 1 | ADD 1 | ADD 0 | STW 1 | ADD 1 | ADD 0
813
824(1) 824(2) 824(3)
SUB 1 | STW 1 | STW 0 | ADDK 1 | B 0 | MPY 1 | MPY 1 | ADD 1
812
256-BIT WIDE INSTRUCTION FETCH PACKETS ARRIVE FROM INTERNAL PROGRAM MEMORY
821(1) 821(2) 821(3) 821(4) 822(0) 823(0) 823(1) 824(0)
SUB 1 | LDW 1 | LDW 1 | B 0 | MVK 0 | ZERO 1 | SHL 0 | ADD 1
811
820(0) 820(1) 820(2) 820(3) 820(4) 820(5) 820(6) 821(0)
MPY 1 | MPY 1 | ADD 1 | ADD 1 | STW 1 | STW 1 | ADDK 0 | ADD 1
810
10
FETCH
DISPATCH
DECODE
32
FUNCTIONAL UNIT NOT ACTIVE FOR THIS CYCLE
ADD
MPY
STW
STW
MPY
ADDK
ADD
FUNCTIONAL UNIT L1
FUNCTIONAL UNIT S1
FUNCTIONAL UNIT M1
FUNCTIONAL UNIT D1
FUNCTIONAL UNIT D2
FUNCTIONAL UNIT M2
FUNCTIONAL UNIT S2
FUNCTIONAL UNIT L2
A14 A12 A10 A8 A6 A4 A2 A0
A15 A13 A11 A9 A7 A5 A3 A1
B14 B12 B10 B8 B6 B4 B2 B0
B15 B13 B11 B9 B7 B5 B3 B1
REGISTER FILE A
REGISTER FILE B
DATA 1
DATA 2
DATA MEMORY INTERFACE/CONTROL
16
0 1 2 3 4 5 6 7
8 9 * * *
DATA ADDRESS 1
DATA ADDRESS 2
INTERNAL DATA MEMORY (BTYE ADDRESSABLE)

FIG. 8

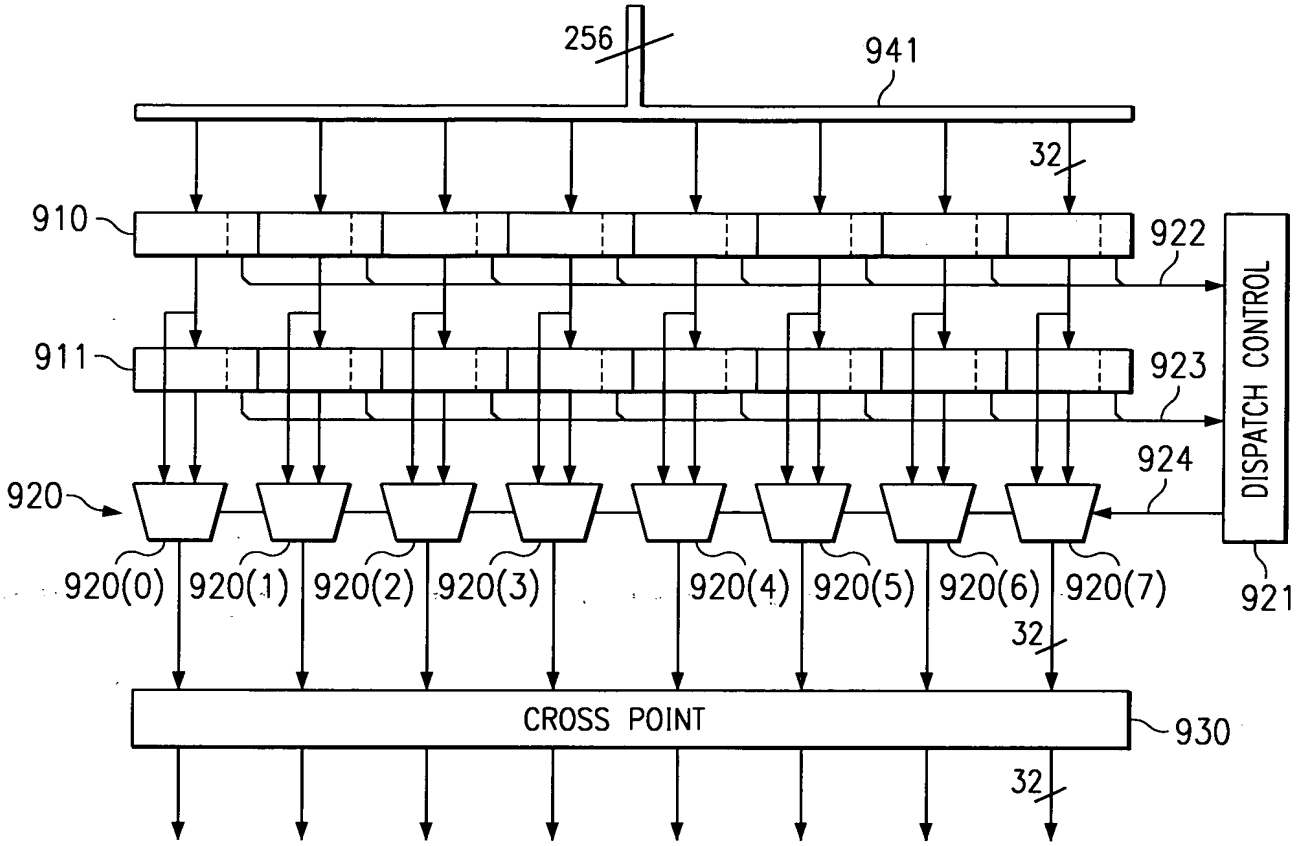


FIG. 9

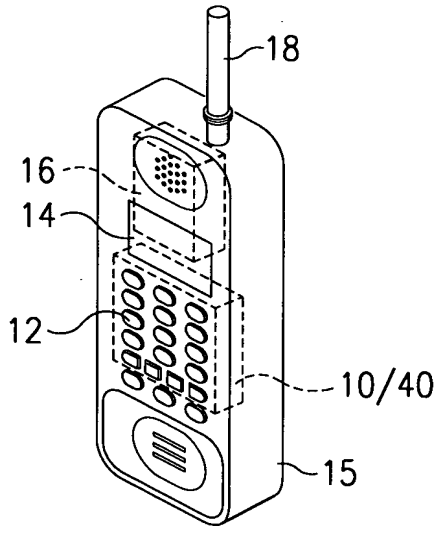


FIG. 11

09/520,760 - 03/08/2000

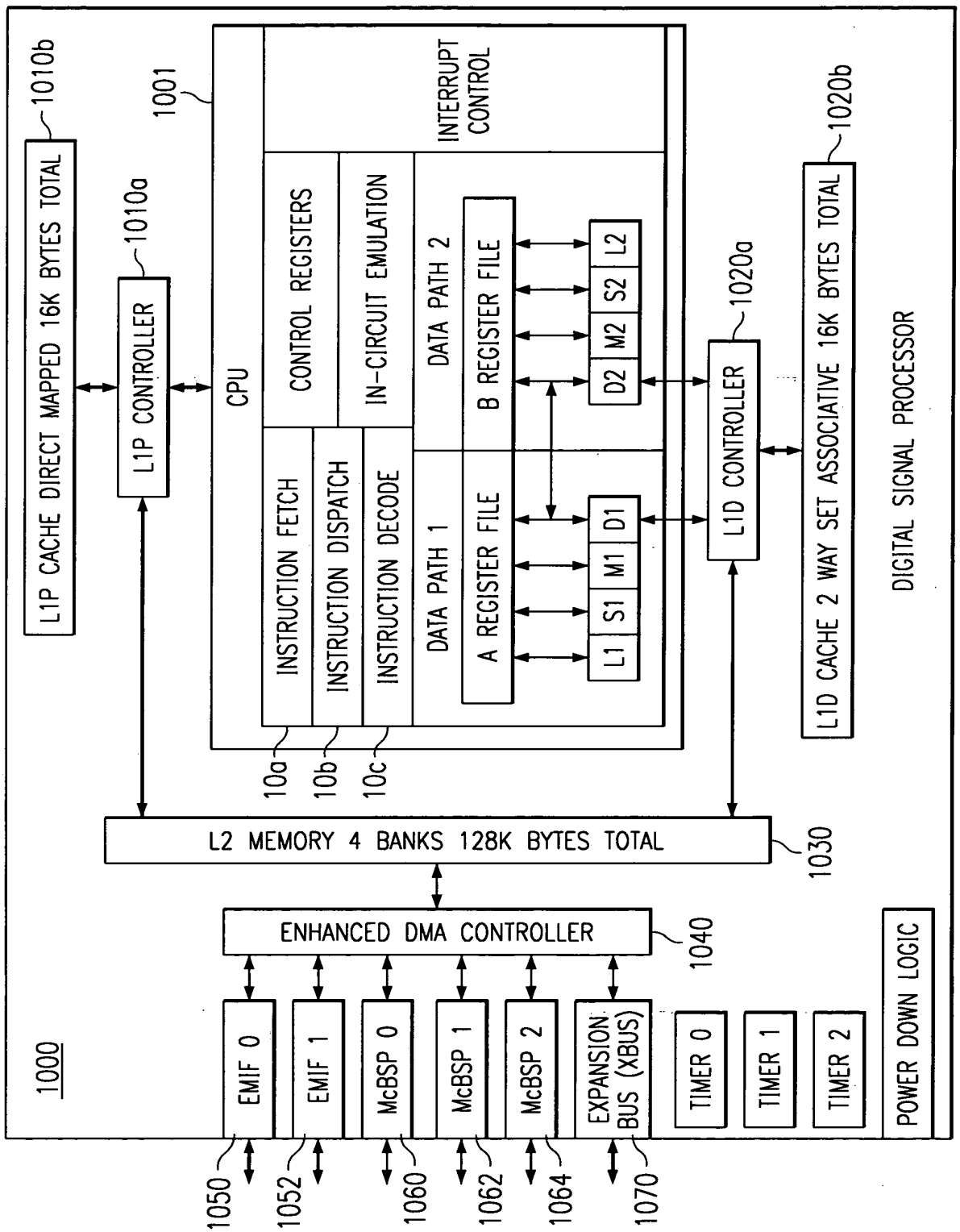

1000
L1P CACHE DIRECT MAPPED 16K BYTES TOTAL
1010b
L1P CONTROLLER
1010a
1001
CPU
INSTRUCTION FETCH
INSTRUCTION DISPATCH
INSTRUCTION DECODE
CONTROL REGISTERS
IN-CIRCUIT EMULATION
INTERRUPT CONTROL
DATA PATH 1
A REGISTER FILE
L1
S1
M1
D1
DATA PATH 2
B REGISTER FILE
D2
M2
S2
L2
10a
10b
10c
L1D CONTROLLER
1020a
L1D CACHE 2 WAY SET ASSOCIATIVE 16K BYTES TOTAL
1020b
DIGITAL SIGNAL PROCESSOR
L2 MEMORY 4 BANKS 128K BYTES TOTAL
1030
ENHANCED DMA CONTROLLER
1040
EMIF 0
EMIF 1
McBSP 0
McBSP 1
McBSP 2
EXPANSION BUS (XBUS)
TIMER 0
TIMER 1
TIMER 2
POWER DOWN LOGIC
1050
1052
1060
1062
1064
1070

FIG. 10